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A Simulated Study of 65 nm CMOS 2GHz Front-End Preamplifier Circuit for Optical Fiber Applications

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ABSTRACT

In this research a new design of the transimpedance amplifier (TIA) with the current mirror was employed by the technique (65nm). The TIA consists of a common gate transistor amplifier (CG TIA) and a common source amplifier as an input stage with local active feedback with a second stage of a current mirror and local active feedback to increase gain. In order to verify the performance of the proposed TIA, a circuit simulation was carried out in the LT spice program using coefficients with the technique (65nm CMOS). The simulation results indicate that the interfacial impedance gain is (41 dBΩ) at a bandwidth frequency of (2.0 GHz-3dB) for an input capacitor of (100 fF) and an input referred noise current spectral density of (14 pA/√Hz) and a power consumption value of (0.091 mw) at an applied voltage (1V). The main focus of this research is low consumption of power and voltage compared to another research.

Keywords: Common-gate (CG) amplifier, Common-source (CS) amplifier, Active feedback, Current mirror.

INTRODUCTION

In a typical optical communication system, the most important function of the receiver is to convert the weak current signal to a larger voltage signal, so an amplifier must be needed in the front end of an optical receiver, and the most important specifications of it should include low input current noise, high and adequate bandwidth and accurate transimpedance gain (Toumazou and Park, 1998) and (Vanisri and Toumazou, 1993). Contemporary Metal Oxide Semiconductor (CMOS) transimpedance amplifier (TIA) is widely used, because of its low input impedance, low-cost wide bandwidth and low input-referred noise current. Common-source (CS) amplifier with shunt feedback is used topology, however, the input parasitic capacitance (C_{in}), which consists of the parasitic capacitance of photodiode, the electrostatic discharge (ESD) circuit and input passive attenuation device (PAD) primarily constrains the noise performances in such TIA and bandwidth. The second widely used topology is the so-called common-gate (CG) (Toumazou *et al.*,1998). The advantages of the CG topology are the very wide bandwidth and the low input impedance of the common-gate input transistor, which make the amplifier bandwidth less sensitive to the input parasitic capacitance (Razavi, 2000). An inductor less modified Regulated Cascode (RGC) TIA was investigated (Taghavi *et al*., 2015). A CMOS Regulated Common-Gate (RCG) TIA based on elliptic filter approach was introduced (Salhi *et al*., 2018) as a compact design, while a low power current mirror TIA was demonstrated for 10 Gbps optical communications (Zohoori *et al*., 2018). The aim of this research is to obtain a low power consumption during the operation of the circuit). In addition, no direct current can pass from V_{dd} to ground as a CMOS appreciable current can rise during switching transients and a current exists only during small fraction of time during device operation (Pimbley *et al.*,1989).

Main Transimpedance Amplifier Concepts

Common-Gate Amplifier

An amplifier stage with low input impedance is the common-gate (CG) (for field effect devices). Ignoring second-order effects in the transistors for present, the input resistance of each stage is approximately equal to $1/g_m$, where g_m represents the transconductance of the input transistor. The right choice of the bias current regarding transistor M_1 device dimensions leads to a relatively low input resistance, in which the input bandwidth can be maximized. The low-frequency circuit shown in Fig. (1) is a typical representation for CG input stage (Razavi, 2012).

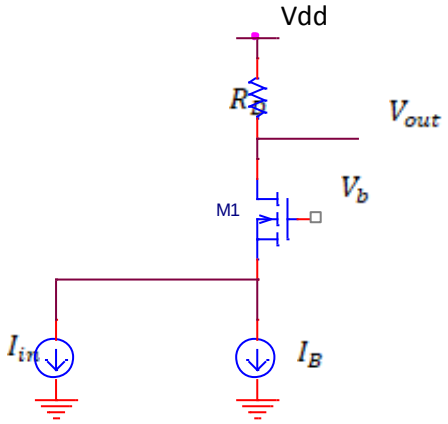

Fig. 1: Basic Common-Gate Circuit Diagram (Razavi, 2012).

Taking into account, channel-length modulation as well as body effect and assuming I_B is an ideal current source, a small-signal equivalent circuit of the CG stage can be assembled as in Fig. (2). The transimpedance gain is $R_T = R_D$, since all of the input current I_{in} flows through resistor R_D (Razavi, 2012).

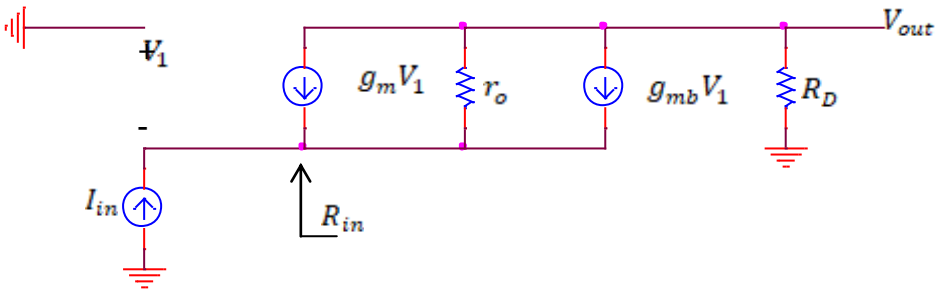

Fig. 2. Small signal model of common gate stage (Razavi, 2012).

To work out the input resistance $-V_1/I_{in}$, the current through r_o is equal to $I_{in} + g_m V_1 + g_{mb} V_1$. By summing the voltage drops across r_o and R_D and having the result equals to $-V_1$, it is obtained as:

$$(I_{in} + g_m V_1 + g_{mb} V_1) r_o + I_{in} R_D = -V_1 \qquad (1)$$

Thus, $R_{in} = -V_1/I_{in}$ and hence,

$$R_{in} = \frac{r_o + R_D}{1 + (g_m + g_{mb}) r_o} \qquad (2)$$

Common-Source (CS) Amplifier

In Fig. (3), in the common source amplifier configuration, the input is introduced to the gate and the output measured at the drain. Transistor M_1 converts the input voltage changes to (proportional) drain current changes in a small signal model, while load resistor R_D (transforms) the drain current to an output voltage. If channel-length modulation is ignored, the small-signal representation in Fig. (3) yields $V_{in} = V_1$ and $V_{out} = -g_{m1} V_1 R_D$ (Razavi, 2006).

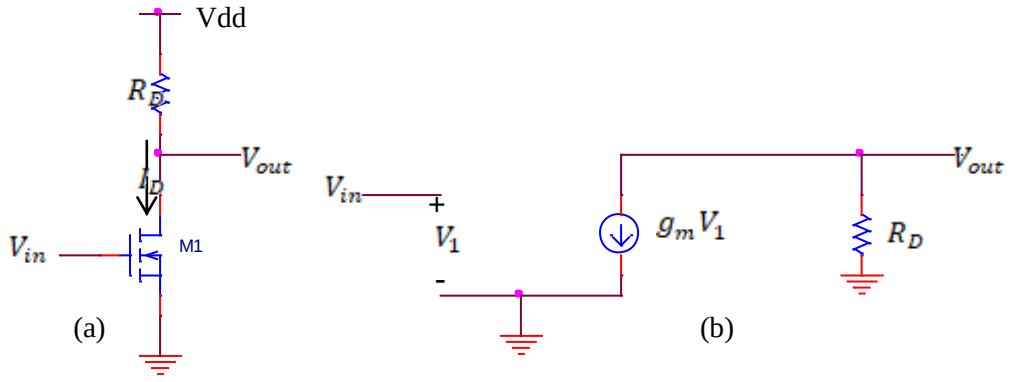

Fig. 3: a: Common source stage. b. small signal mode (Razavi, 2006).

Current Mirror Topology

The current mirror topology is an electrical circuit that is mainly designed to maintain constant current within a circuit network, as the circuits have recently been reduced in volume. The size of today's transistors is available at the nanoscale with the effect of channel length modulation is taken into account ((King and Leblebici, 2003), (Allen and Holbers, 2011) and (Suman, 2018)).

In Fig. (4), it is noted that the drain-gate voltage of the ambient transistor M_1 is zero, therefore, the channel does not exist at the drain, and the two transistors M_1 and M_2 operate in the saturation region if the overdrive voltage is positive, as the current that flows in the drain of M_1 is mirrored to the drain of M_2 (Gray *et al.*, 2001).

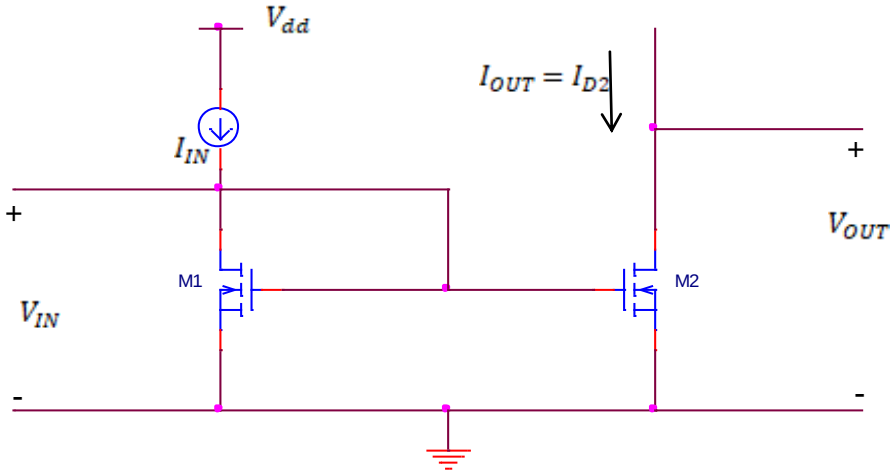

Fig. 4: Current mirror topology

The Design of Proposed (TIA) Circuit

In this section, the design of the transimpedance amplifier (TIA) structure with current mirror implemented in a low-voltage (1V) and 65 nm CMOS technology as shown in Fig. (5). The proposed TIA topology involves a common-gate (CG) TIA and common-source (CS) TIA, with active feedback resistor and the current mirror to increase the gain in transimpedance. This work is a development of previous research (Phang, 2001). In this work, LT spice Software was used to simulate the proposed transimpedance amplifier. It is based upon PSpice circuit solver engine which enable circuits to be solved on mathematical conversion point. This work is a development of earlier work (Al-Kawaz and Alsheikhjader, 2020) and (Alsheikhjader, 2020).

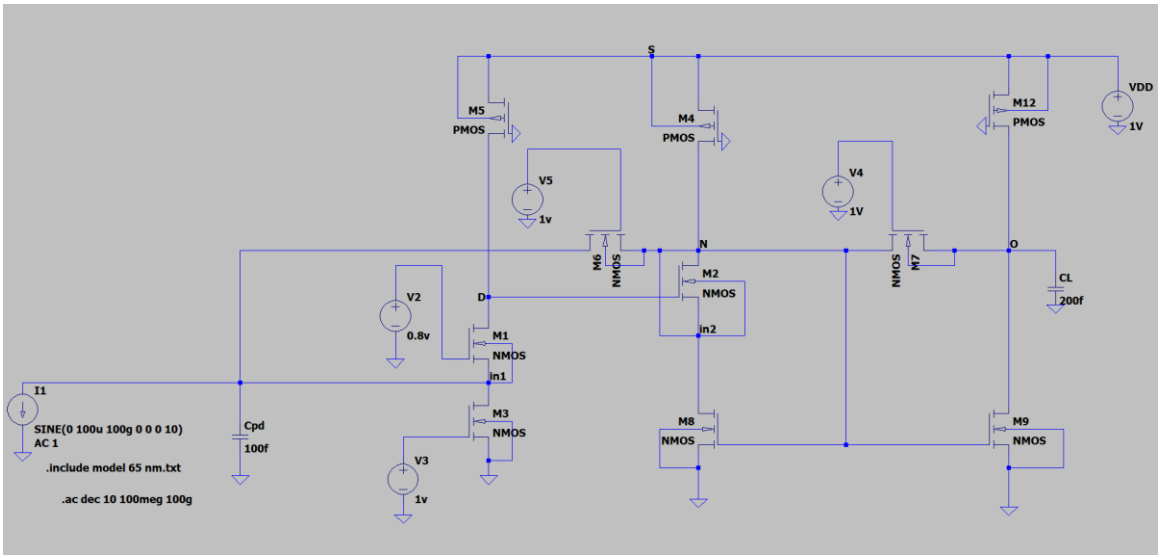

Fig. 5: Proposed low-voltage TIA

When the light applied on the photodiode, it will transform the light into a suitable current. The built-in input capacitance (100fF) was connected parallel to the photodiode. The input capacitance

is inversely proportional to the bandwidth frequency as the input capacitance increases, the bandwidth cut off frequency reduced and this is due to the photodiode limitations that have direct influence on input capacitance. And also, the circuit output is connected to another built-in capacitance (200fF output load capacitance). The current from the photodiode would then move through the M_1 NMOS transistor representing the common-gate (CG) amplifier operating in the saturation region. So, the signal exiting in the drain terminal for M_1 passes through and amplified by the M_2 common source structure arriving at node N in which it is fed back to the input through transistor M_6. Part of the signal at node N enters a second stage current-mirror topology. Gate-to-source voltages of transistor M_8 and M_9 are set to be equal in order to mirror the drain current of transistor M_2 into the second stage output node. At the point of output node, there is second local active feedback in the form of transistor M_7 through which a fraction of the signal is feedback to node N and ultimately to the input of the second stage through the source terminal of transistor M_2. It is important to notice that the signal feedback through transistor M_7 is partitioned to the source of transistor M_2 as well as through the transistor M_6 back to the input of the first stage. Fig. (5) also shows that there are three PMOS transistors M_4, M_5 and M_{12} which function as "current sources" as used to maintain the current stability in the circuit. Now, after reviewing the circuit operation, the internal variables for each type of NMOS and PMOS transistor are shown in (Table 1).

Table 1: Parameters of NMOS and PMOS transistors

n-channel	W / L	p-channel	W / L
M_1	6.17	M_4	1.3
M_2	6.17	M_5	1.3
M_6	6.17	M_{12}	1.3
M_7	6.17		
M_8	3.25		
M_9	3.25		
M_3	1.3		

Input Stage TIA Gain Derivation

Now, the circuit's transimpedance gain can be derived according to Fig. (5) according to the general formula (Staric and Margan, 2006):

$$\frac{v_o}{v_i} = -A_{(s)} = -A_o \frac{s_o}{s - s_o} = -A_o \frac{\omega_o}{s + \omega_o} \qquad (3)$$

s is the complex frequency variable., A_o is the amplifier open DC gain. s_o is the amplifier real dominant pole, so that: $-s_o = \omega_o = 2\pi f_o$ as f_o is the open loop cutoff frequency.

The sum of currents at the v_i input node is:

$$i_i = \frac{v_i}{\frac{1}{s\,c_i}} + \frac{v_i - v_o}{\frac{1}{\frac{1}{r_{o6}} + s\,c_{f6}}} \qquad (4)$$

Leading to the inclusion of the closed loop voltage gain A in relation to input and output voltages

$$i_i = -\frac{v_o}{A} s c_i - \frac{v_o \left(\frac{1}{A} + 1\right) r_{o6}}{1 + s\,c_{f6}\,r_{o6}} \qquad (5)$$

Further development of above equation can be put forward by using equation (3) as the final transimpedance gain equation for the input stage appears to have a third order denominator.

$$\frac{v_o}{i_i} = \frac{-A_o\ \omega_\circ \dfrac{(1 + s\ c_{f6}\ r_{o6})}{c_i\ c_{f6}\ r_{o6}}}{s^3 + \dfrac{s^2 c_i(1 + \omega_\circ\ c_{f6}\ r_{o6})}{c_i\ c_{f6}\ r_{o6}} + \dfrac{s(\omega_\circ\ c_i + r_{o6})}{c_i\ c_{f6}\ r_{o6}} + \dfrac{\omega_\circ\ r_{o6}(1 + A_o)}{c_i\ c_{f6}\ r_{o6}}} \quad (6)$$

Overall TIA Gain Derivation

It is known that gain, bandwidth and noise are important requirements for circuit design with design pre-requisites such as supply voltage and input capacitance influencing each.

Since the TIA gain of the first stage is defined as in v_{o1}/I_{in1} , the current gain takes a new expression as in:

$$\frac{v_{o1}}{I_{in1}} = \frac{Z_{o1}\ I_{o1}}{I_{in1}} \rightarrow \frac{I_{o1}}{I_{in1}} = \frac{v_{o1}}{I_{in1}} \cdot \frac{1}{Z_{o1}} \quad (7)$$

The output impedance of the first stage is represented by:

$$Z_{o1} = r_{o2}//r_{o6}//r_{o4}//r_{o7} \quad (8)$$

From equations (6) and (7), the final current gain expression becomes:

$$\frac{I_{o1}}{I_{in1}} = \frac{-A_o\omega_\circ \dfrac{(1 + s\ c_{f6}\ r_{o6})}{c_i\ c_{f6}\ r_{o6}}}{s^3 + s^2 A + sB + C} \cdot \left[\frac{1}{r_{O2}} + \frac{1}{r_{O4}} + \frac{1}{r_{O6}} + \frac{1}{r_{O7}}\right] \quad (9)$$

Note that:

$$A = \frac{c_i(1 + \omega_\circ\ c_{f6}\ r_{o6})}{c_i\ c_{f6}\ r_{o6}}\ ; B = \frac{(\omega_\circ\ c_{i+} r_{o6})}{c_i\ c_{f6}\ r_{o6}}; C = \frac{\omega_\circ\ r_{o6}(1 + A_o)}{c_i\ c_{f6}\ r_{o6}}$$

Following on the current mirror small signal derivation, the TIA gain for the second stage is derived as:

$$\frac{v_{o2}}{I_{in2}} = \frac{y_{f7} - g_{m9}}{\dfrac{y_N\ y_{in}\ y_{f7}}{g_{m2}} + \left[\dfrac{y_{f7}}{g_{m2}}\ y_{in}\ (y_N + y_L) + y_N\ y_L\right] + \left[g_{m9}\ y_{f7}\ \dfrac{y_{in}}{g_{m2}} + g_{m8}\ y_{f7} + y_{f7}(y_L + y_N)\right] + (g_{m8} + g_{m9})y_{f7}} \quad (10)$$

Current mirror stage admittances are defined as y_{in} as the input admittance, y_L as the load admittance, y_N as node N admittance and y_{f7} as the second local active feedback admittance. Given the fact that $I_{o1} = I_{in2}$, and according to equation (11), the final expression (V_{o2}/I_{n1}) for the overall TIA gain of the proposed amplifier is improvised. In this section, the overall TIA gain is based upon multiplying gain of the first stage in equation (9) by the second stage gain of equation (10).

$$\frac{v_{o2}}{I_{in1}} = \frac{I_{o1}}{I_{in1}} \cdot \frac{v_{o2}}{I_{in2}} \qquad (11)$$

TIA Bandwidth Derivation

To find the bandwidth, the TIA's input resistance is derived in order to comply with the following general bandwidth equation.

$$f - 3dB = \frac{1}{2\,\pi\, R_{in}\, c_{in}} \qquad (12)$$

The small signal model of Fig. (2) can have the following derivation for the circuit input resistance which in line with literature (Razavi, 2012).

$$R_{in} = \frac{r_{o5}\,(r_{o1}+r_{o6}) + r_{o1}\, r_{o6}}{(g_{m1} + g_{mb1}).r_{o1}\, r_{o6}} \qquad (13)$$

The TIA input capacitance is expressed as $c_{in} = c_{pd} + c_{db3} + c_{sb1}$. By substituting this input capacitance and input resistance of equation (13) into equation (12), the TIA bandwidth equation is given as:

$$f_{-3dB} = \frac{(g_{m1} + g_{mb1})\,.\, r_{o1}\, r_{o6}}{2\,\pi[r_{o5}(r_{o1}+r_{o6}) + r_{o1}\, r_{o6}].\,[c_{pd} + c_{db3} + c_{sb1}]} \qquad (14)$$

Proposed TIA Gain Results and Discussion

The simulated proposed TIA circuit indicated the importance of low power consumption demand by the industry with regard to low voltage devices. Short channel effects did not have that much of an impact on the data stated in Table 3. Despite the moderate TIA gain of 41 dBΩ at 2 GHz of bandwidth, an extremely low magnitude of 0.091 mW (power consumption) is reported. However, an extremely low input referred noise current spectral density is obtained. After entering and simulating these variables for the NMOS and PMOS transistors, we obtained optimal results as shown in the low voltage (1V) supply (Table 2 and 3) concluding: high gain, wide bandwidth, low power consumption, and low noise at high frequencies.

Table 2: Power consumption of each transistor

Transistors	Power Consumption
M1	58.174nw
M2	7.4516nw
M3	1.297μw
M4	29.979μw
M5	30.039μw
M6	222.81nw
M7	135.61nw
M8	11.707nw
M9	31.236nw
M12	29.915μw
Total	0.091 mw

Table 3: Main characteristics of proposed TIA

CMOS Technology	**65nm CMOS (Vth:0.2 V NMOS and -0.9 V PMOS)**
Input Capacitance	100fF
Supply Voltage	1 V
Gain	41 dBΩ
Bandwidth	2 GHz
Power Consumption	0.091 mw
Input-Referred Noise	14 pA/√Hz

In Fig. (6), a simulated transimpedance gain versus frequency is reported, in which the f_{-3dB} bandwidth of 2 GHz is confirmed at a gain of 41 dBΩ. It is important to point out however, that the low input capacitance of 100 fF (in simulation) did have an important role to play in having a relatively wide bandwidth. The dominant pole of this frequency response does appear at the bandwidth point. The effect of pole zero may not have a direct effect on the cut off frequency of the circuit, however, the dominant pole in Fig. (6) is due to the direct effect of the input capacitance given earlier. Most effective is the input photodiode capacitance which appears in parallel with the input stage (i.e., the source of transistor M_1) in a form of common-gate configuration.

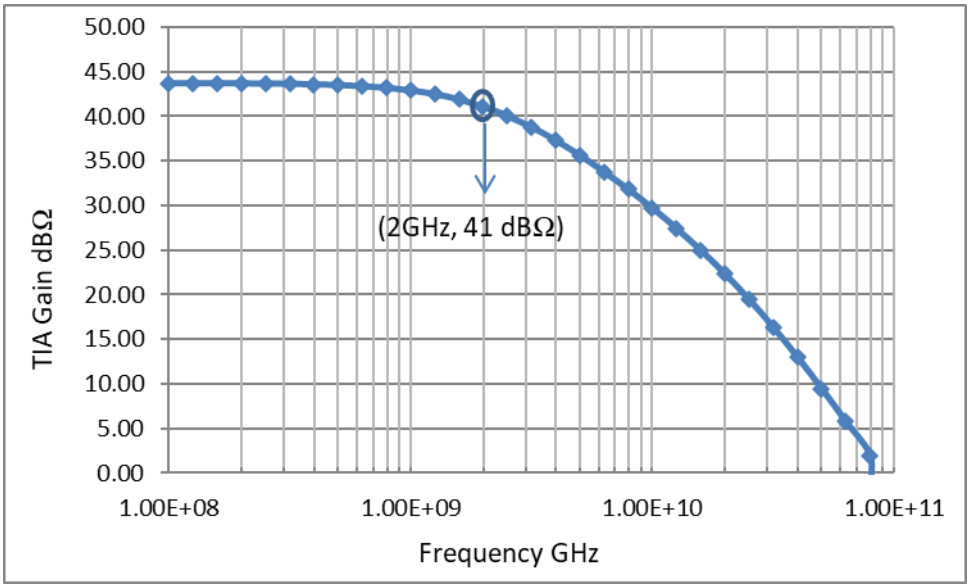

Fig. 6: Simulated TIA gain versus frequency.

A DC sweep biasing of transistor M_1 gate was carried out from (0.8V-1V) and an output voltage swing range is obtained as in Fig. (7). The reason behind changing the DC biasing of this particular transistor is the fact that transistor M_1 source is the circuit input terminal which decides how far the signal can be amplified initialy, controls circuit bandwidth through input parasitic capacitance as given earlier. Furthermore, the source of transistor M_1 repsents the other end of the local active feedback of transistor M_6, hence affecting negative feedback mechanism greatly. Needless to say that transistor M_7 which is the local active feedback of the second stage also connected through node N to transistor M_6. A DC biasing sweep effectively changing the overdrive voltage $(V_{GS} - V_{TH})$ of transistor M_1 and this means that the drain current is influenced greatly

which in turn affects the voltage gain of the common gate input stage and subsequently the overlall voltage gain of the circuit.

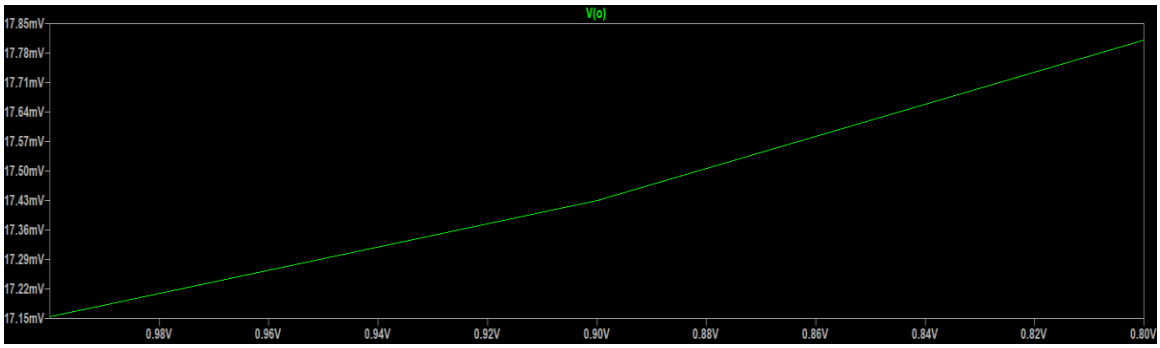

Fig. 7: DC sweep over biasing voltage of transistor M_1 from (0.8V – 1V).

Transient analysis were perfomed in simulation for the output voltage swing in time domain configuration in which a maximum time period of 100 ps was examined. This analysis corresponds to the frequency response of Fig. (6). The output voltage swing is an indication of how the transimpedance gain will progress throughout the time domain range. In Fig. (8), This type of waveform is due to the fact that the signal from input to output faces a series-parallel built-in parasitic capacitances at high frequencies. These capacitances resist any abrupt change in voltage across them and therefore a (discontinuous) change in voltage requires an infinite current and that is physically not possible. As a result and because of this abrupt change in voltage, the current through these parasitic capacitances changes instantaneously.

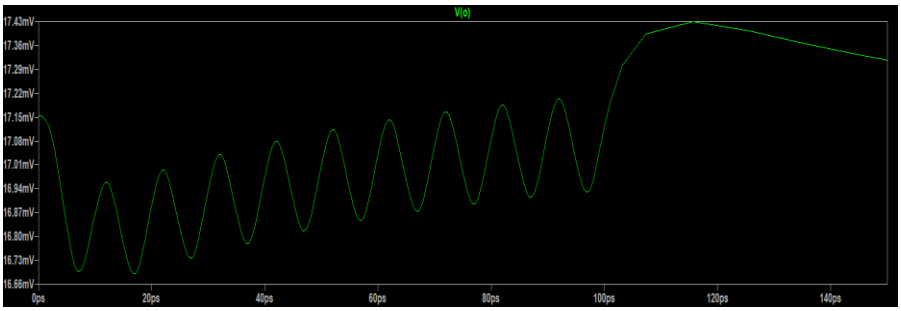

Fig. 8: Simulated time domain transient analysis of the output voltage signal.

Noise Analysis and Results

The noise characteristics of the transimpedance amplifier regarding the noise current spectral density referred to input or the corresponding reference noise current spectral density are of great importance for evaluating the sensitivity of the entire front-end optical receiver (Sackinger, 2005), (Vanisri and Toumazou, 1995). And also, a TIA sensitivity is constraint by its noise performance. At high TIA bandwidth, the dominant noise is the thermal noise. Fig. (9) illustrates the noise equivalent circuit model for the closed loop TIA structure.

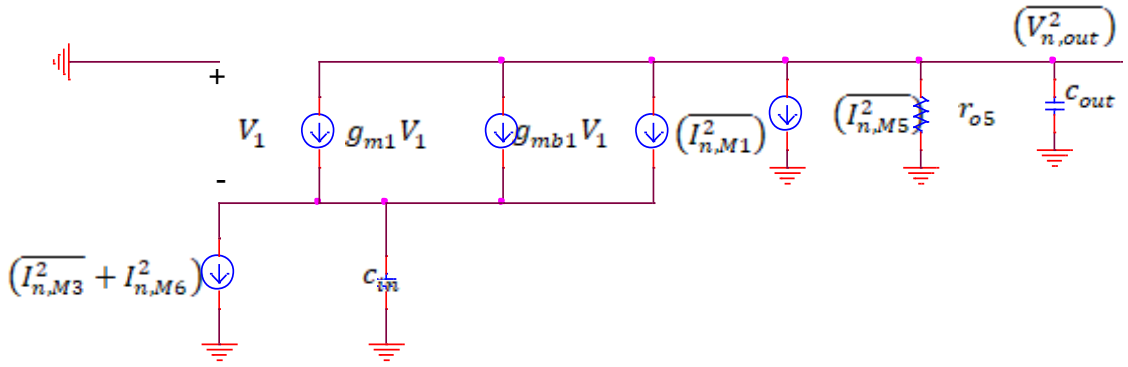

Fig. 9: Noise equivalent model of the proposed TIA.

To derive the total input referred noise current equation, the Kirchhoff voltage law is applied on the noise equivalent model above according to the general formula (Razavi, 2012):

$$v_{n,out} = \frac{-r_{o5}\, c_{in}\, s\, I_{n,M_1}}{(c_{in}\, s + g_{mb1} + g_{m1})(r_{o5}\, c_{out}\, s + 1)} + \frac{I_{n,r_{o5}}\, r_{o5}}{r_{o5}\, c_{out}\, s + 1} \qquad (15)$$

The TIA gain of the first input stage common gate general formula is (Razavi, 2012):

$$\frac{v_{out}}{I_{in}} = \frac{(g_{m1} + g_{mb1})\, r_{o5}}{(g_{m1} + g_{mb1} + c_{in}\, s)(r_{o5} c_{out}\, s + 1)} \qquad (16)$$

Dividing equation (15) by the TIA gain given by equation (16), it is obtained as:

$$I_{in} = \frac{-c_{in}\, s}{g_{m1} + g_{mb1}} I_{n,M_1} + \left(\frac{c_{in}\, s}{g_{m1} + g_{mb1}} + 1\right) I_{n,r_{o5}} \qquad (17)$$

Two important features are deduced from above equation (Meyer and Blauschild, 1986). First, Transistor M_1 noise contribution scales in a direct way with input capacitance c_{in} and input frequency. Second, the noise contributed by r_{o5} towards the input node does rise given that $|c_{in}s|$ is comparable to the magnitude of $(g_{m1} + g_{mb1})$ (Razavi, 2012). The total input referred noise current spectral density can be integrated in which it is computed as a noise voltage divided by the mid band gain. An integration of the following function for a frequency from 0 to ∞ is needed.

$$V_{n,out}^2 = \frac{1}{c_{in}^2 - (g_{m1} + g_{mb1})^2\, r_{o5}^2\, c_{out}^2}\left(\frac{-(g_{m1} + g_{mb1})^2}{c_{in}^2(2\pi f)^2 + (g_{m1} + g_{mb1})^2} + \frac{1}{r_{o5}^2\, c_{out}^2(2\pi f)^2 + 1}\right) + \frac{r_{o5}^2\, I_{n,r_{o5}}^2}{r_{o5}^2\, c_{out}^2(2\pi f)^2 + 1}$$
$$+ \frac{1}{c_{in}^2 - (g_{m1} + g_{mb1})^2\, r_{o5}^2\, c_{out}^2}\left(\frac{c_{in}^2}{c_{in}^2(2\pi f)^2 + (g_{m1} + g_{mb1})^2} + \frac{-r_{o5}^2\, c_{out}^2}{r_{o5}^2\, c_{out}^2(2\pi f)^2 + 1}\right) \qquad (18)$$

To deal with the second-order fraction of above equation, (Razavi, 2012).

$$\int_0^{\infty} \frac{4KTRdf}{(2\pi Rcf)^2 + 1} = \frac{KT}{c} \qquad (19)$$

Decomposing the first and third terms of (18) into partial fractions and carrying out the integration with the aid of (19), and if the input pole is assumed to be dominant, i.e., $c_{in}/(g_{m1}+g_{mb1}) \gg r_{o5}\, c_{out}$, then

$$V_{n,out,tot}^2 \approx \frac{KT(g_{m1}\, r_{o5}\, \gamma + 1)}{c_{out}} + \frac{2KT(g_{m1}+g_{mb1})g_{m2}\, r_{o5}^2\, \gamma}{c_{in}} \qquad (20)$$

Since for short- channel MOSFETS,
$\gamma > 1$, it is reasonable to assume that $g_{m1} r_{o5} \gamma \gg 1$. Dividing both sides by r_{o5}^2 yields the total input-referred noise current:

$$I_{n,in,tot}^2 \approx \frac{K\, T\, g_{m1}\, \gamma}{r_{o5}\, c_{out}} + \frac{2KT(g_{m1}+g_{mb1})\, g_{m2}\, \gamma}{c_{in}} \qquad (21)$$

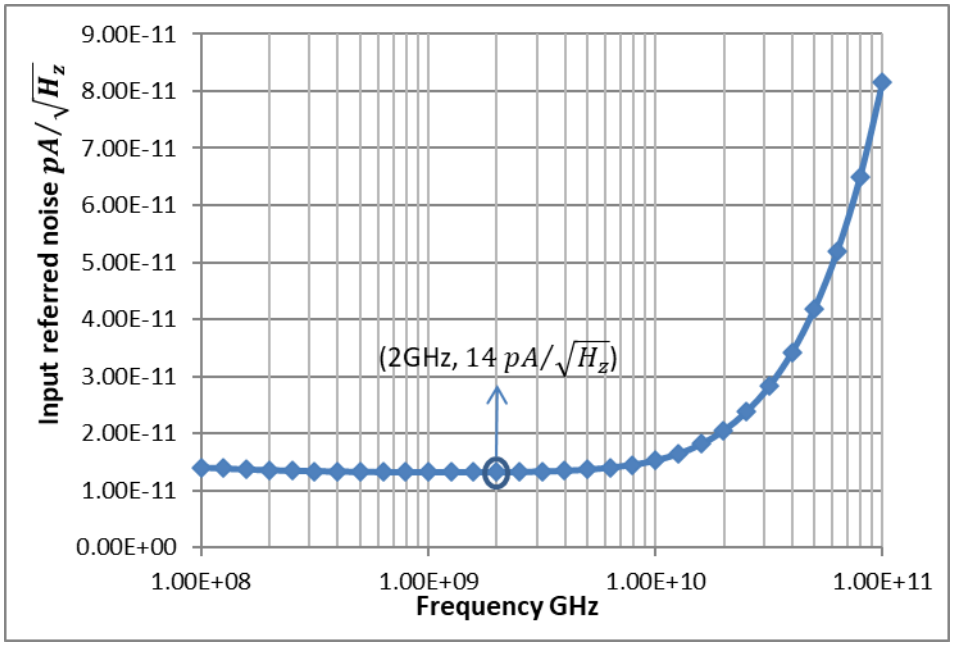

Fig. 10: Simulated input-referred noise of proposed TIA.

Table 4: Performance comparison between the proposed TIA and other design works

Researchers	Technology (CMOS)	Gain (dBΩ)	Bandwidth (GHz)	Power consumption(W)	Input Capacitance(fF)	Supply voltage(V)	Input Noise (pA/√Hz)
(Rakideh *et al.*, 2016)	0.18 μm	58	8.1	34.8 m	300	1.8	15
(Chen *et al.*, 2013)	0.18 μm	46	8	31.5 m	250	1.8	40
(Taghavi *et al.*, 2015)	0.13 μm	50.1	7	7.5 m	250	1.5	31.3
(Andre and Jacobus., 2016)	0.13 μm	54	11.5	45 m		1.5	6.8
(Honda *et al.*, 2016)	0.13 μm	72	38.4	261 m		3.3	14.8
(Hui *et al.*, 2011)	0.35 μm	54.2	2.3	58 m	500	3.3	18.8
(Seifouri *et al.*, 2017)	0.18 μm	59	7.9	18 m	300	1.8	23
(Chen *et al.*., 2017)	0.13 μm	83.7	32.1	150 m		3.3	
(Chen *and Yang.*, 2016)	0.18 μm	55-69	1	6 m		1.8	9.33
This Work 2022	65 nm	41	2	0.091 m	100	1	14

CONCLUSION

In this work, a new topology is reported for the transimpedance amplifier (TIA) for use in optical fiber application. A TIA with low voltage, high gain, extremely low power consumption and low noise is designed based on the novel topology of CG_CS stage with NMOS local active feedback followed by a current mirror stage with a second NMOS local active feedback. The proposed design is simulated with 1V 65nm CMOS technology. The simulation results show the transimpedance gain of 41 dBΩ with a bandwidth of around 2.0 GHz and photodiode parasitic capacitance of 100 fF. Average input-referred noise current spectral density is equal to 14 pA/√Hz.

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دراسة عبر محاكاة دائرة بتقنية CMOS 65nm عند تردد 2GHz لواجهة نهائية لمكبر اولي يستخدم في تطبيقات الالياف البصرية

الملخص

في هذا البحث تم استخدام تصميم جديد لمكبر الممانعة البينية (TIA) مع استخدام دائرة مرآة التيار بتقنية (65 نانومتر). الهدف من هذا البحث هو الحصول على استهلاك منخفض للطاقة أثناء تشغيل الدائرة. يتكون TIA من مكبر ترانزستور بوابة مشترك (CG TIA) ومكبر مصدر مشترك كمرحلة إدخال مع تغذية استرجاع محلية فعالة يتبعه مرحلة ثانية من مرآة التيار وتغذية استرجاعية محلية فعالة ثانية لزيادة الربح. من أجل التحقق من أداء TIA المقترح، تم إجراء محاكاة للدائرة في برنامجٍ LT Spice باستخدام معاملات مع التقنية (65nm CMOS). تشير نتائج المحاكاة إلى أن ربح الممانعة البينية هو (41 ديسيبل) بتردد عرض نطاق (2.0 جيجا هرتز) عند (− 3 ديسيبل) بسعوية دخل شاردة للدايود الضوئي قدرها (100 فيمتو فاراد) وكثافة طيفية لتيار الضوضاء المشار إليها تبلغ (14بيكو امبير لكل جذر هرتز) وقيمة استهلاك الطاقة (0.091 ملي واط) بجهد مطبق (1 فولت). التركيز الرئيسي لهذا البحث هو الاستهلاك المنخفض للطاقة والجهد مقارنة بالبحوث الأخرى.

الكلمات الدالة: مكبر البوابة المشتركة (CG)، مكبر المصدر المشترك (CS)، تغذية الاسترجاع الفعالة، مرآة التيار.